

file:///C:/Users/.../Downloads/3064at44.bsd

Contents: [Dobrica Pavlinu's random unstructured stuff]

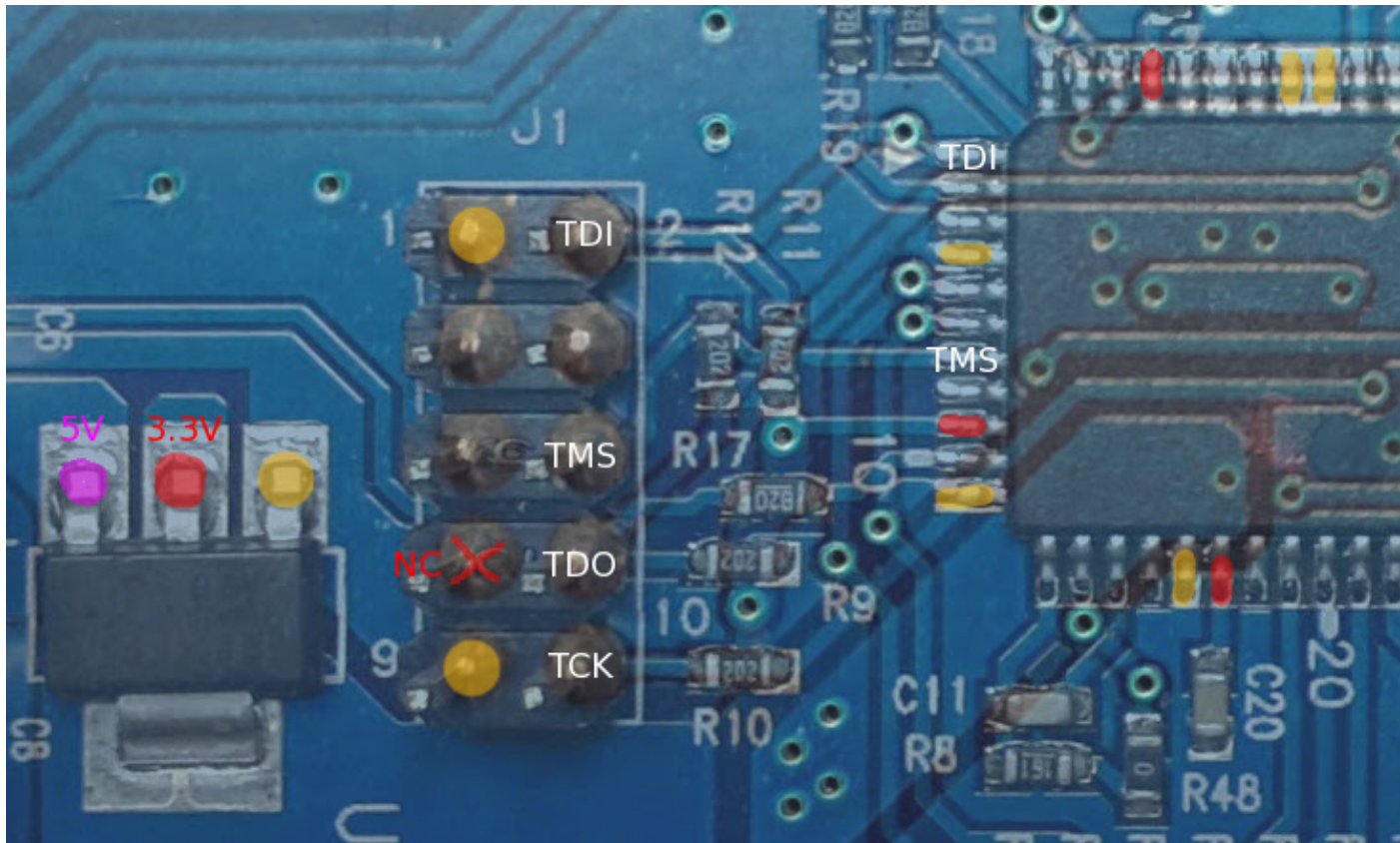
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X300 dongle

- Altera EPM3064A TC44-10N <ftp://ftp.altera.com/outgoing/download/bsd/3064at44.bsd>
- LD1117A L33AUD

JTAG

I took picture of both sides of board, corrected it using perspective tool in gimp and added layers with VCC (5V and 3.3V) and GND (checked with unimer continuity test).



JTAG pinout doesn't match silkscreen designation of pin 1 (it's rotated). It also doesn't have VCC pin connected, so you need to supply 5V power via other means (I used PS/2 connector).

Bus Blaster jtag try:

```
jtag> cable jtagkey vid=0x0403 pid=0x6010 interface=0
Connected to libftd2xx driver.
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00010111000001100100000011011101 (0x170640DD)
  Manufacturer: Altera (0x0DD)
  Part(0):      EPM3064A (0x7064)
  Stepping:    1
  Filename:    /usr/local/share/urjtag/altera/epm3064a/epm3064a
```

```
jtag> print chain
No. Manufacturer      Part              Stepping Instruction      Register
-----
* 0 Altera            EPM3064A         1      BYPASS                    BYPASS
```

```
# IMPORTANT: load signal aliases for this package
jtag> include /usr/local/share/urjtag/altera/epm3064a/t44
```

```
# get values of all pins
```

```
jtag> instruction SAMPLE/PRELOAD
jtag> shift ir
jtag> shift dr
jtag> dr
01001011101011101001011101001001001001011111111010111010
111010010010010111010010010010010010010010010010010010010
```

```

010010010010010010010010010010010010010010010010010010010010010
010010010010010111010111010010
(0x000000000000000000000000000000024924924924975D2)

```

```
jtag> print chain
```

No.	Manufacturer	Part	Stepping	Instruction	Register
* 0	Altera	EPM3064A	1	SAMPLE/PRELOAD	BSR

```

jtag> get signal IO2
IO2 = 1
jtag> get signal IO3
IO3 = 1
jtag> get signal IO43
IO43 = 1
jtag> get signal IO44
IO44 = 1

```

```
# toggle single pin
```

```

jtag> instruction EXTEST
jtag> shift ir

```

```
jtag> print chain
```

No.	Manufacturer	Part	Stepping	Instruction	Register
* 0	Altera	EPM3064A	1	EXTEST	BSR

```

jtag> set signal IO10 out 0
jtag> shift dr

```

```
# re-read values of all pins
```

```

jtag> instruction SAMPLE/PRELOAD
jtag> shift ir
jtag> shift dr
jtag> get signal IO10
IO10 = 0

```

SVF programming

```

jtag> svf /blue-zfs/FPGA/Altera-x300/x300_dongle/output_files/dongle1.svf stop progress
detail: Parsing 20/520 ( 3%)warning: unimplemented mode 'ABSENT' for TRST
detail: Parsing 520/520 (100%)detail:
detail: Scanned device output matched expected TDO values.

```

VHDL to toggle pins

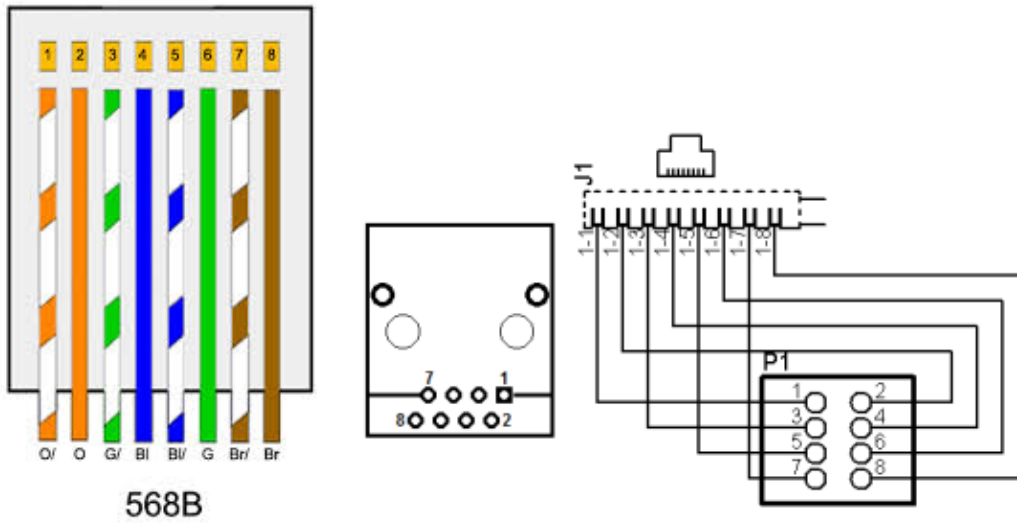
Toggle pins on all four sides of CPLD and create additional two images with all one and all zero for easy test where pin is

[dongle1.vhd](#)

Then I connected logic analyzer on pins and tried different svf files (all-0, all-1, left, bottom, right, top) to locate which pin change depending on image loaded. To isolate pins I used EXTEST and

toggled pins.

RJ45

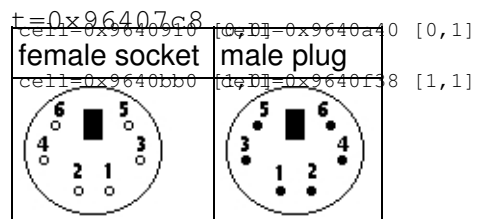


pin	pull	cable
1	0	GND
2	1	VGA?
3	0	IO?
4	1	VGA?
5	0	IO?
6	1	VGA?
7	0	IO10
8	0	5V

PS2

PS2

<http://www.computer-engineering.org/ps2protocol/>



6-pin Mini-DIN (PS/2):

- 1 - Data
- 2 - Not Implemented
- 3 - Ground

- 4 - Vcc (+5V)
- 5 - Clock
- 6 - Not Implemented

Keyboard (left, purple)

t=0x9642608 cell=0x9642610 [0,1]

pin	IO
1 (data)	IO43
5 (clock)	IO44

Mouse (right, green)

t=0x9642f10 cell=0x9642f10 [0,1]

pin	IO
1 (data)	IO34
5 (clock)	IO35

Audio jack

R2R D2A

all measurements are done on Hantek 2090 with 500mV/div setting which may account for some accuracy errors

channel 1

t=0x9644068 cell=0x9644070 [0,2]

state	min	max
off	64.17 mV	95.54 mV
IO23	1.664 V	1.696 V
IO22	864 mv	895 mV
IO21	472 mV	503 mV
IO20	283 mV	299 mV
IO19	189 mv	221 mV

channel 2

t=0x9645a98 cell=0x9645aa0 [0,2]

state	min	max
off	3.3	50 mV
IO33	113 mV	144 mV
IO31	207 mV	254 mV

cell=0x361600641501-0x361600641501 [4,2]		
IO28	395 mV	442 mV
cell=0x361600641501-0x361600641501 [5,2]		
IO27	803 mV	850 mV
cell=0x361600641501-0x361600641501 [6,2]		
IO25	1.603 V	1.635 V