



Hi3515 H.264 Encoding and Decoding Processor

Key Features

CPU Core

- ARM926EJ
- I-cache 16 KB, D-cache 16 KB
- I-TCM 2 KB
- Built-in MMU, supporting multiple open operating systems such as VxWorks, Linux, WinCE, and PalmOS
- Up to 400 MHz operating frequency

Video Encoding/Decoding

- H.264 main profile encoding/decoding
- H.264 baseline profile encoding/decoding
- JPEG/MJPEG baseline encoding/decoding

Video Encoding/Decoding Performance

- Overall performance of real-time H.264 encoding/decoding: 4-channel D1
- Maximum resolution for the H.264 encoding/decoding: 1280x1024@30fps
- Dual streams are supported during simultaneous H.264 encoding and decoding:
 - 240fps CIF encoding+240fps QCIF encoding+120fps CIF decoding@NTSC
 - 200fps CIF encoding+200fps QCIF encoding+100fps CIF decoding@PAL
 - 240fps CIF encoding+120fps QCIF encoding+240fps CIF decoding@NTSC
 - 200fps CIF encoding+100fps QCIF encoding+200fps CIF decoding@PAL
- 1.3 megapixels@30fps to 3 megapixels@10fps
- 3 megapixels@10fps JPEG snapshot
- CBR/VBR bit rate control, ranging from 16 kbit/s to 20 Mbit/s

Graphics Processing

- Video input de-interlace (pre-processing)
- Video output de-interlace (post-processing)
- Anti-flicker processing for video and graphics outputs
- Video and graphics scaling
- OSD overlapping of four areas after pre-processing
- Hardware graphics overlapping of four layers (video layer, graphics layer 1, graphics layer 2, and cursor layer) after video post-processing
- Video blending up to four areas
- Motion detection

Audio Encoding/Decoding

- Encoding and decoding audios with multiple channels and protocols through software

Security Engine

- Various encryption and decryption algorithms such as AES, DES, and 3DES through hardware
- Digital watermark technology

Video Interfaces

- Input:
 - Supporting 4-channel BT.656 YCrCb 4:2:2 interfaces, 8 bits, 27/54/108 MHz
 - Supporting 1-channel standard SMPTE296M and BT.1120 HD timings
 - Supporting two digital camera interfaces with the maximum resolution of 1280x1024@30fps, 1600x1200@20fps, and 2048x1536@10fps
- Output:
 - Multiple video output interfaces
 - VGA x 1 + CVBS x 1
 - Typical VGA output resolutions: 1024x768@60fps, 1280x720@60fps, 1280x1024@60fps, 1440x900@60fps, and 1366x768@60fps
 - BT.656 digital output

Audio Interfaces

- Two I²S interfaces. Each supports up to 16-channel 8-bit or 16-bit audio cascade inputs
- Multiple sampling frequencies such as 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz
- Multiple sampling precisions such as 8 bits, 16 bits, and 32 bits

Peripheral Interfaces

- Four UART interfaces
- IR interface, I²C interface, SPI master/slave interface, and GPIO interface
- SDIO 2.0 interface, up to 32 GB
- Two USB 2.0 host interfaces with the hub function
- MAC interface, supports 10 Mbit/s or 100 Mbit/s MII interface in full-duplex or half-duplex mode

SATAII Interfaces

- Two SATA 2.6 interface, up to 3 Gbps
- External SATA PM expansion device
- eSATA

External Memory Interfaces

- One DDR2 SDRAM interface
 - 32-bit or 16-bit data width, 200 MHz
 - Up to 256 MB
- NOR flash interface
 - 8-bit data width
 - Two CSs, each up to 32 MB
- NAND flash interface
 - 8-bit data width
 - Supporting SLC, MLC, and 1-bit, 4-bit, and 8-bit ECC
 - Up to 8 GB
- Boot from the NOR flash or NAND flash

SDK

- SDK based on Linux 2.6.24



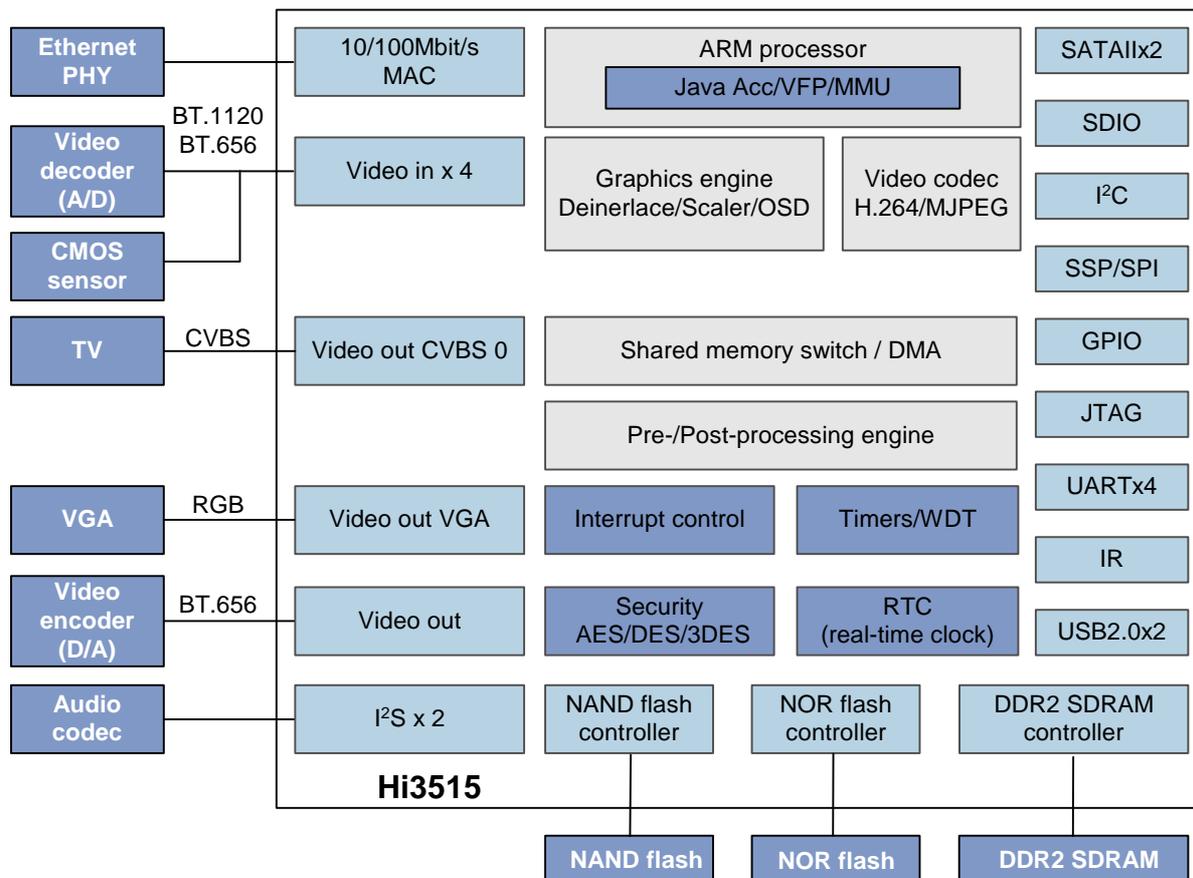
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- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
 - 1000 mW typical power consumption
 - Multiple-level power-saving modes
- Operating voltage
 - Core voltage: 1.0 V
- Package
 - 441-pin TFBGA package
 - 0.8 mm ball pitch, 19 mm x 19 mm
- IO voltage: 3.3 V.
- Tolerance voltage: 5 V
- Voltage of the DDR2 SDRAM interface: 1.8 V
- Operating temperature: -20–85°C

Functional Block Diagram



The Hi3515 is a high-performance communications media processor based on the ARM9 processor core and the video hardware acceleration engine. With the frequency of up to 400 MHz, the ARM9 meets the increasing demands in multiple software applications such as the DVR, DVS, and IP camera. The 200 MHz DDR2 SDRAM interface provides sufficient bandwidth and powerful capability for data processing. The Hi3515 supports H.264 and MJPEG encoding/decoding under multiple protocols and dual-stream encoding. The encoding/decoding performance is up to 120fps D1@NTSC or 100fps D1@PAL. Therefore, the Hi3515 supports the optimal 4-channel CIF or 8-channel DVR solution that features high performance and low cost. In addition, the Hi3515 has various video input or output interfaces such as the CVBS, HD VGA, and BT.1120 interfaces. With the maximum resolution of 1280x1024@60fps, the Hi3515 enables the digital surveillance products to bring customers an excellent video experience with better image quality.

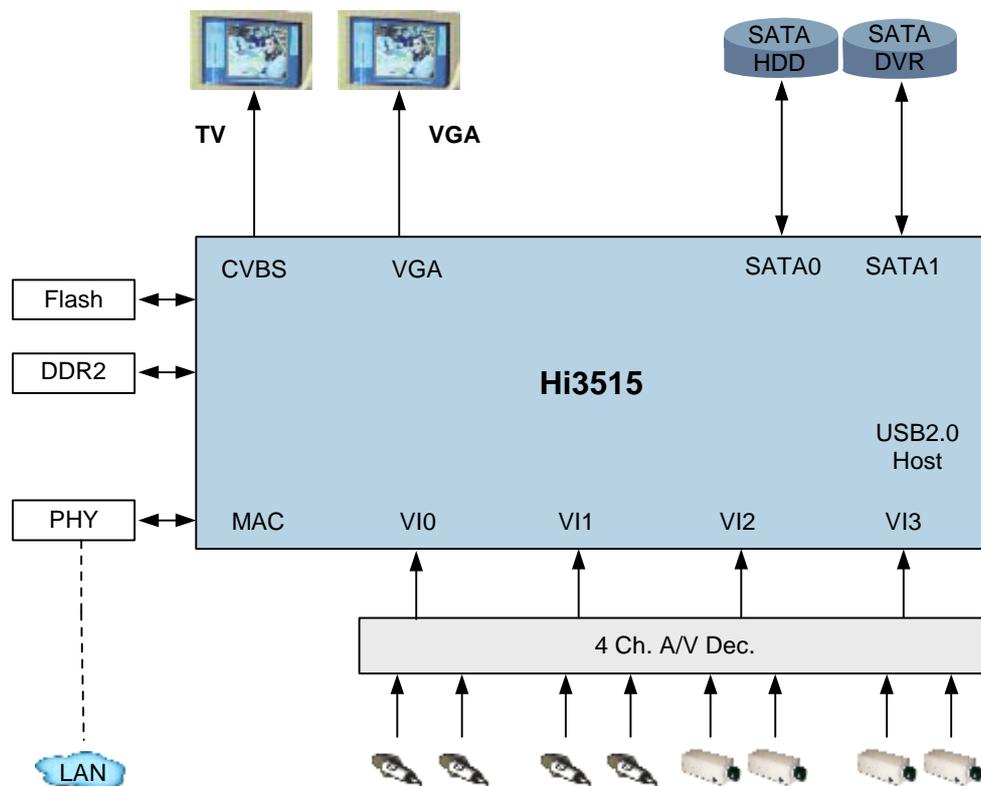


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Application Fields and Typical Application Diagrams

4-Channel DVR Solutions

- 4-channel CIF DVR with a single Hi3515
 - 1280 x 1024 VGA output
 - D1 spot CVBS display and output
 - 4-channel CIF video recording in real time
 - 4-channel CIF network transferring in real time
 - 4-channel CIF decoding playback in real time





Hi3515 H.264 Encoding and Decoding Processor

- 8-channel CIF DVR with a single Hi3515
 - 1280 x 1024 VGA display and output
 - D1 spot CVBS display and output
 - 8-channel CIF video recording in real time
 - 8-channel QCIF network transferring in real time
 - 8-channel CIF decoding playback in real time

